

**WHAT IS CLAIMED IS:**

1. An apparatus for decoding a variable length code, comprising:
  - a pre-decoding unit for receiving a data bitstream and generating a first selection signal or a second selection signal for selecting a look-up table address register according to a code value of the data bitstream, wherein M is a natural number;
  - a shifter for shifting the data bitstream by a predetermined number of bits in response to one of the first selection signal and the second selection signal and a predetermined continuous node signal;
- 10 a set of first through M-th look-up table address registers, each look-up table address register comprising a LOC address designating a K-bit LOC table value stored in a memory, wherein K is a natural number;
- 15 a selector for selecting an output of the first through M-th look-up table address registers and outputting a selected output in response to one of the first selecting signal and second selection signal;
- 20 a memory controller for receiving the output of the selector, generating a third selection signal for selecting a LOC table value and a terminal value corresponding to the LOC table value in response to the predetermined continuous node signal, or generating a fourth selection signal for selecting a predetermined fixed length code stored in the memory in response to a predetermined symbol address signal, wherein the LOC table value and the terminal value are stored in the memory, and the terminal value is used to obtain a predetermined symbol address;
- 25 a memory for storing LOC table values, terminal values, and fixed length codes, outputting a LOC table value and a terminal value in response to the third selection signal, and outputting a fixed length code in response to the fourth selection code; and

a memory searcher for receiving the LOC table value and the terminal value that are output from the memory and L-bits of the data bitstream, determining whether the L bits of the data bitstream designate a terminal node or a continuous node using a LOC information table stored therein, generating a 5 continuous node signal or a symbol address signal based on a result of the determination, receiving the fixed length code output from the memory, and outputting the fixed length code, wherein L is a natural number.

2. The apparatus of claim 1, wherein the pre-decoding unit comprises:

10 a first pre-decoder for receiving the data bitstream and when sequential 0s or 1s exist in a set of most significant bits (MSBs) of the data bitstream, generating the first selection signal for selecting the look-up table address register from the set of first through M-th look-up table address registers according to a number of sequential 0s or 1s; and

15 a second pre-decoder for receiving the data bitstream and generating the second selection signal for selecting the look-up table address register from the set of first through M-th look-up table address registers using N bits in the set of MSBs of the data bitstream, wherein N is a natural number.

20 3. The apparatus of claim 1, wherein the shifter shifts the data bitstream by 3 bits in response to the predetermined continuous node signal.

4. The apparatus of claim 1, wherein the memory controller comprises:

25 an offset register for receiving the selected output and storing the selected output until a next selected output is received from the selector;

an adder for generating the third selection signal for selecting values from a LOC table stored in the memory by adding an output of the offset register and a predetermined next LOC address;

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a LOC address register for generating the predetermined next LOC address in response to the continuous node signal; and

a symbol address register for generating the fourth selection signal for selecting the fixed length code in response to the symbol address signal.

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5. The apparatus of claim 4, wherein the next LOC address is a sum of a current LOC address and a number of non-terminal nodes in a current LOC up to a current node.

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6. The apparatus of claim 1, wherein the predetermined symbol address is a sum of a terminal value corresponding to a current LOC table value and a number of terminal nodes in a current LOC before a current node.

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7. The apparatus of claim 1, wherein the LOC information table stored in the memory searcher comprises node types indicating whether a node designated by the variable length code is a terminal node, a continuous node, or an invalid node, each node type comprising  $N*2^L$  LOC information bits, and LOC information bits for each node type are expressed using four formats A, B, C, and D, each format comprising N bits.

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8. The apparatus of claim 7, wherein in the LOC information table stored in the memory searcher, when the variable length code is 0, 1, 00, 01, 10, or 11, a node type designated by the variable length code is a terminal node; and when the variable length code is one of 000 through 111, a node type designated by the variable length code is one of the terminal node, the continuous node, and the invalid node, and

wherein in a case where N is 2 and L is 3, when the variable length code is 0, an upper 8 bits of the LOC information bits are expressed as ABBB; when the variable length code is 1, a lower 8 bits of the LOC information bits are

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expressed as ABBB; when the variable length code is 00, an upper 4 bits of the LOC information bits are expressed as AB; when the variable length code is 01, the LOC information bits from an upper fifth to eighth places are expressed as AB; when the variable length code is 10, the LOC information bits from an upper ninth to twelfth places are expressed as AB; when the variable length code is 11, the LOC information bits from an upper thirteenth to sixteenth places are expressed as AB; and when the variable length code is one of 000 through 111, LOC information bits for a terminal node designated by the variable length code are expressed as A, LOC information bits for a continuous node designated by the variable length code are expressed as C, and LOC information bits for an invalid node designated by the variable length code are expressed as D.

9. The apparatus of claim 7, wherein in the LOC information table stored in the memory searcher, when the variable length code is 0 or 1, a node type designated by the variable length code is a terminal node; and when the variable length code is one of 00 through 11, a node type designated by the variable length code is one of the terminal node, the continuous node, and the invalid node, and

wherein in a case where N is 2 and L is 2, when the variable length code is 0, an upper 4 bits of the LOC information bits are expressed as AB; when the variable length code is 1, a lower 4 bits of the LOC information bits are expressed as AB; and when the variable length code is one of 00 through 11, LOC information bits for the terminal node designated by the variable length code are expressed as A, LOC information bits for the continuous node designated by the variable length code are expressed as C, and LOC information bits for the invalid node designated by the variable length code are expressed as D.

10. The apparatus of claim 1, wherein each LOC table value stored in the memory comprises LOC information bits corresponding to node types designated by each variable length code of a current LOC in the LOC information table.

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11. The apparatus of claim 1, wherein the selector is a multiplexer.

12. A method of decoding a variable length code using a variable length code decoding apparatus comprising a set of first through M-th look-up table address registers each look-up table address register comprising a predetermined LOC address, the variable length code decoding apparatus comprising a memory storing a LOC table, which comprises K-bit LOC table values corresponding to each LOC address and predetermined terminal values corresponding to each LOC address, and fixed length codes, and the variable length code decoding apparatus comprising a memory searcher storing a LOC information table comprising information referred to for decoding a variable length code, wherein M is a natural number and K is a natural number, the method comprising:

20 (a) receiving a data bitstream and generating one of a first selection signal and a second selection signal for selecting a look-up table address register from the set of the first through M-th look-up table address registers according to a code value of the data bitstream;

25 (b) selecting an output of the first through M-th look-up table address registers in response to one of the first selection signal and the second selection signal;

(c) generating a third selection signal for selecting a LOC table value and a terminal value corresponding to the LOC table value from the LOC table stored in the memory by adding the output selected in step (b) and a predetermined

next LOC address, the terminal value being used to obtain a predetermined symbol address;

(d) selecting the LOC table value and the terminal value from the LOC table in response to the third selection signal;

5 (e) determining whether L bits of the data bitstream designates a terminal node or a continuous node using the LOC information table based on the selected LOC table value and the selected terminal value, which are output from the memory, to generate a continuous node signal or a symbol address signal, wherein L is a natural number;

10 (f) generating the predetermined next LOC address used for selecting the LOC table value in response to the continuous node signal;

(g) generating a fourth selection signal for selecting a fixed length code in response to the symbol address signal; and

15 (h) selecting a fixed length code from the memory and outputting the fixed length code, in response to the fourth selection signal.

13. The method of claim 12, wherein step (a) comprises:

(a1) when sequential 0s or 1s exist in a set of most significant bits (MSBs) of the data bitstream, generating the first selection signal for selecting the first through M-th look-up table address register according to the number of sequential 0s or 1s;

(a2) generating the second selection signal for selecting one from the first through M-th look-up table address register using N bits in the set of MSBs of the data bitstream, wherein N is a natural number; and

25 (a3) shifting the data bitstream by a predetermined number of bits in response to one of the first selection signal and the second selection signal and the continuous node signal.

14. The method of claim 12, wherein the next LOC address is a sum of a current LOC address and a number of non-terminal nodes in a current LOC up to a current node.

5 15. The method of claim 12, wherein the symbol address is a sum of a terminal value corresponding to a current LOC table value and a number of terminal nodes in a current LOC before a current node.

10 16. The method of claim 12, wherein the LOC information table stored in the memory searcher comprises node types indicating whether a node designated by the variable length code is a terminal node, a continuous node, or an invalid node, each node type comprising  $N*2^L$  LOC information bits, and LOC information bits for each node type are expressed using four formats A, B, C, and D, each format comprising N bits.

15 17. The method of claim 16, wherein in the LOC information table stored in the memory searcher, when the variable length code is 0, 1, 00, 01, 10, or 11, a node type designated by the variable length code is a terminal node; and when the variable length code is one of 000 through 111, a node type designated by the variable length code is one of the terminal node, the continuous node, and the invalid node, and

20 25 wherein in a case where N is 2 and L is 3, when the variable length code is 0, an upper 8 bits of the LOC information bits are expressed as ABBB; when the variable length code is 1, a lower 8 bits of the LOC information bits are expressed as ABBB; when the variable length code is 00, an upper 4 bits of the LOC information bits are expressed as AB; when the variable length code is 01, the LOC information bits from an upper fifth to eighth places are expressed as AB; when the variable length code is 10, the LOC information bits from an upper ninth to twelfth places are expressed as AB; when the variable length code is 11,

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the LOC information bits from an upper thirteenth to sixteenth places are expressed as AB; and when the variable length code is one of 000 through 111, LOC information bits for a terminal node designated by the variable length code are expressed as A, LOC information bits for a continuous node designated by  
5 the variable length code are expressed as C, and LOC information bits for an invalid node designated by the variable length code are expressed as D.

18. The method of claim 16, wherein in the LOC information table stored in the memory searcher, when the variable length code is 0 or 1, a node type designated by the variable length code is a terminal node; and when the  
10 variable length code is one of 00 through 11, a node type designated by the variable length code is one of the terminal node, the continuous node, and the invalid node, and

15 wherein in a case where N is 2 and L is 2, when the variable length code is 0, an upper 4 bits of the LOC information bits are expressed as AB; when the variable length code is 1, a lower 4 bits of the LOC information bits are expressed as AB; and when the variable length code is one of 00 through 11, LOC information bits for the terminal node designated by the variable length code are expressed as A, LOC information bits for the continuous node designated by  
20 the variable length code are expressed as C, and LOC information bits for the invalid node designated by the variable length code are expressed as D.

19. The method of claim 12, wherein each LOC table value stored in the memory comprises LOC information bits corresponding to node types  
25 designated by each variable length code of a current LOC in the LOC information table.